Examensarbete utfört i Elektroniksystem
vid Tekniska högskolan i Linköping
av

Robert Kihlberg

LiTH-ISY-EX--08/4241--SE

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Algorithms for Noise Shaping and Interleaving of Digital to Analog Converters

Examensarbete utfört i Elektroniksystem vid Tekniska högskolan i Linköping av

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This thesis investigates the possibilities of interleaving multiple Digital to Analog converters in a high speed environment. Algorithms for interleaving and noise shaping as well as filters are tailored for high frequency operation.

In the first part of the thesis, algorithms are evaluated and models to simulate errors are created. It was concluded that DAC interleaving is feasible to reach high sample rates. Interleaving or parallelization of the $\Sigma\Delta$ noise shaper proved to not be feasible for the specific application due low oversampling and high speed operation.

The second part of the thesis consists of measurements on a custom SP Devices development board. These tests confirm that interleaving of DACs works as intended and that it is possible to increase the output bandwidth beyond the one of a single DAC.
Abstract

This thesis investigates the possibilities of interleaving multiple Digital to Analog converters in a high speed environment. Algorithms for interleaving and noise shaping as well as filters are tailored for high frequency operation.

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All knowledgeable and helpful people at SP Devices for comments, suggestions and proof reading assistance.

My family and friends for valuable feedback and motivation.

Till Mormor.
## Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Full Form</th>
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<tbody>
<tr>
<td>DAC</td>
<td>Digital to Analog Converter</td>
</tr>
<tr>
<td>dB</td>
<td>Decibel</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>ENOB</td>
<td>Effective Number of Bits</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field-Programmable Gate Array</td>
</tr>
<tr>
<td>FIR</td>
<td>Finite Impulse Response</td>
</tr>
<tr>
<td>$f_s$</td>
<td>Sampling frequency</td>
</tr>
<tr>
<td>Gb</td>
<td>Gigabit</td>
</tr>
<tr>
<td>GB</td>
<td>Gigabyte</td>
</tr>
<tr>
<td>GET</td>
<td>Gigabit Ethernet Transport</td>
</tr>
<tr>
<td>GS</td>
<td>Giga Sample</td>
</tr>
<tr>
<td>LVDS</td>
<td>Low Voltage Differential Signaling</td>
</tr>
<tr>
<td>MS</td>
<td>Mega Sample</td>
</tr>
<tr>
<td>NTF</td>
<td>Noise Transfer Function</td>
</tr>
<tr>
<td>OSR</td>
<td>Oversampling Rate</td>
</tr>
<tr>
<td>PANDA</td>
<td>Pulse And Noise shaping Digital to Analog converter</td>
</tr>
<tr>
<td>PC</td>
<td>Personal Computer</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>QAM</td>
<td>Quadrature Amplitude Modulation</td>
</tr>
<tr>
<td>RAM</td>
<td>Random Access Memory</td>
</tr>
<tr>
<td>RRC</td>
<td>Root Raised Cosine</td>
</tr>
<tr>
<td>RTZDAC</td>
<td>Return-to-Zero Digital to Analog Converter</td>
</tr>
<tr>
<td>SCM</td>
<td>Sub Carrier Modulation</td>
</tr>
<tr>
<td>SIAM</td>
<td>Silicon Analog to Millimeter-wave Technology</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal to Noise Ratio</td>
</tr>
<tr>
<td>SNDR</td>
<td>Signal to Noise and Distortion Ratio</td>
</tr>
<tr>
<td>STF</td>
<td>Signal Transfer Function</td>
</tr>
<tr>
<td>USB</td>
<td>Universal Serial Bus</td>
</tr>
<tr>
<td>W-CDMA</td>
<td>Wideband Code Division Multiple Access</td>
</tr>
</tbody>
</table>
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Chapter 1

Introduction

This document was written as the report of a Master of Science thesis in Applied Physics and Electrical Engineering at the Department of Electrical Engineering at Linköping Institute of Technology. The task was performed at Signal Processing Devices AB.

1.1 Background

The European research projects SIAM (Silicon Analog to Millimeter-wave Technology) and 100GET (100Gigabit Ethernet Transport) are focused on building blocks for a 100Gbit Ethernet optical link. A critical part of this link is the Digital to Analog Converter (DAC), which is optimized for the system specification. The system uses sub carrier modulation (SCM) which splits the data into a set of independent channels. In this way, the 100Gbit data stream is transmitted on a set of relatively narrow channels. For this implementation, a set-up with 1.75GHz bandwidth on each channel is tested. Each SCM channel can be viewed as a 1.75GHz system. The signal bandwidth in the DAC is thus 1.75GHz.

In the SIAM-project, SP Device’s contribution is PANDA, a Pulse And Noise shaping Digital to Analog converter. The pulse shaping is in principle interpolation and filtering, which is placed on chip for limiting the data rate in the digital interface. The noise shaping is a Sigma-Delta modulator, which is increasing the dynamic range in the signal band. The data rate is expected to be higher than the maximum possible clock frequency of a chip implementation. Therefore, the architecture is parallelized to increase the throughput.
The DAC development is divided into two projects which are related to each other. One is implementation of the analog blocks and the other is this project, development of the algorithms.

1.2 Purpose

The purpose of this thesis is to develop an algorithm for a time-interleaved Digital to Analog converter (DAC) to the 100GET project with as low hardware requirements as possible.

1.3 Methodology

The project is divided into two main parts; algorithm development and measurements.

The algorithm part consists of developing a set of discrete blocks to carry out oversampling, filtering, modulation and noise shaping. These blocks are finally combined and simulations are carried out to match the required specifications.

The measurement part consists of implementing the model in Verilog and conducting tests and measurements on a custom development board.

1.4 Disposition

Chapter 2 - Proposed Solution introduces ideas and approaches to solving the task of a high speed data converter.

Chapter 3 - Digital to Analog Conversion covers time interleaving of DACs and its purpose.

Chapter 4 - Noise shaping covers interleaving and parallelization of a \(\Sigma\Delta\)-modulator.

Chapter 5 - Filtering discusses the digital pulse and noise shaping filters in the design and their purposes.
Chapter 6 - Algorithm Conclusions concludes the creation of the algorithm model.

Chapter 7 - Measurements are carried out on hardware and analysis of the interleaving techniques are tested.

Chapter 8 - Conclusions summarizes the thesis and discusses the results.
Chapter 2

Proposed Solution

This section covers the pre-study of the thesis work where a possible solution is discussed.

2.1 Overview

The main purpose of this thesis is to design a system for the 100GET project that converts the 6-bit input data to an analog output signal with at least 4 effective number of bits (ENOB). The analog signal has a bandwidth requirement of 1.75GHz which results in a minimum sample rate of 3.5GS/s. Sequential signal processing at these frequencies require dedicated hardware and simple operations, if achievable at all. To ease the requirements on the hardware, parallelization and minimization of the execution path will be carried out.

2.2 Specification

The proposed solution is to use a set of digital to analog converters (DAC) in parallel, clocked at a lower rate than the system. To relax the requirements on the DACs even more, it was suggested to reduce the output to 4 bits, compared to the 6 bits of the input data. The requirements specify that the output signal needs to have at least an ENOB of 4. As a result, oversampling and noise shaping was considered a necessity. Both of these increases the demands on the digital processing and it was Therefore suggested to investigate the possibilities to parallelize the algorithms.
The proposed system was setup according to the principle shown in Fig. 2.1. Initially, the input data rate of 3.5 GS/s is oversampled by a factor 4 to 14 GS/s. Following the oversampling is a set of filters consisting of an interpolation filter and a root raised cosine (RRC) filter to handle inter symbol interference. Further on is the signal divided into four parallel paths as inputs to the parallel Sigma-Delta (ΣΔ) modulator which is performing noise shaping of the signal. As can be seen in the figure, this is where the signal is quantized from 6 bits to 4. Finally, a set of interleaved DACs are operating with a clock offset compared to each other to form the analog output. The condensed requirements are found in Tab. 2.1.

\[
\text{SNR}_{\text{dB}} = 6.02 \cdot \text{ENOB} + 1.76 \quad (2.1)
\]

SNDR is the acronym for Signal to Noise and Distortion ratio and takes distortion tones into account, aswell as SNR. The SNDR requirement originates from the ENOB with the approximate relation given by Eq. 2.1 [6]. Since SNDR is a more continuous measure than ENOB, the former will be used throughout this report.
Chapter 3

Digital to Analog Conversion

This chapter explains the structure of the proposed interleaved DAC structure. It also presents how the model was created, error sources considered and simulation results.

3.1 DAC Interleaving

The reason to attempt to interleave a set of digital to analog converters is to increase the output bandwidth of the combined setup. The requirements specify that the output signal should have a signal bandwidth of 1.75GHz and an output sample rate of 14GS/s. This is faster than any commercial off the shelf DAC and it is therefore necessary to develop a parallel architecture.

The idea is to use \( M \) parallel Return-to-Zero-DACs (RTZDAC), each operating at one \( M:\text{th} \) of the sample rate and with a phase offset of \( 2\pi/M \). A RTZDAC outputs its analog value during the positive clock edge and returns to zero during the negative edge, which is illustrated in Fig. 3.1. For this study \( M = 4 \). One realizes that each sample is held for \( M/2 \) clock cycles at the high frequency because of the lower clock speeds of each individual DAC.
This results in an overlap of the analog output which can be modelled with the difference Eq. 3.1a and its corresponding transfer function in the frequency domain, Eq. 3.1b. A simple schematic for the combined DAC structure can be seen in Fig. 3.2.

\[
y(n) = x(n) + x(n - 1) \quad (3.1a)
\]
\[
H(z) = \frac{1 + z}{z} \quad (3.1b)
\]

The overlap caused by the interleaving results in a zero at half the sampling frequency. This is because every other sample is the negated value of the previous one and the DAC outputs will cancel each other out. If for example DAC 1 outputs 1 and DAC2 outputs -1, the combined output will be 0. This is is illustrated in Fig. 3.3, where the red line symbolizes the ideal frequency response of the transfer function in relation to the simulated DAC.
response. Since the system is oversampled, the signal band, illustrated by the green color in Fig. 3.3, will not be affected by this.

3.2 DAC Modelling

The proposed solution consists of four DACs operating with a clock offset of $\pi/2$. However, differences in manufacturing will lead to different properties of each DAC, even if they originate from the very same silicon wafer. This so-called mismatch will affect the performance of the circuit in many different ways [6]. To be able to quantify the effect of these variances, the model splits each clock period into 32 pieces, allowing precise manipulation of different behaviours.

3.3 Error simulations

This section covers a variety of errors identified to be obstructive to the interleaving of DACs. The simulations cover errors introduced by differences in synchronization between the DACs, differences in the length of the ON-periods, gain mismatch between the DACs and cycle to cycle jitter.

3.3.1 Clock Skew

The proposed solution uses four DACs with $\pi/2$ phase offset between each DAC. The main issue with the synchronization is to align the clock to the second DAC exactly $\pi/2$ off phase compared to DAC one. High speed
DACs use differential (LVDS) clock inputs and thus are the inverted clocks created by just swapping the clock input wires.

Table 3.1 displays different noise levels of the DAC system when one DAC is delayed compared to when a pair of DACs are delayed. This is also illustrated in Fig. 3.5, where the blue and green lines are the noise levels of $0 - 1.750\text{GHz}$ and $0 - 2.625\text{GHz}$ respectively. Even though the SNDR inside the signal band is well within the specification, there are images of higher frequencies outside of the band. This behaviour is illustrated in Fig. 3.6, where the clock of one DAC is skewed. The effect of this is that an image appear just outside of the spectrum, which would require a very steep analog filter to remove. If at the same time the DAC with the inverted clock is also skewed by the same amount, the image is moved further up in the spectrum causing no harm to the interesting frequency band. Since these tones occur when the clock offset between DAC 1 and 3 as well as 2
3.3 Error simulations

and 4 differ from $\pi$, great care need to be taken in aligning the inverted clocks.

Figure 3.5: Noise levels from different DAC delays

Figure 3.6: DAC image outside of the frequency band. Signal frequency 1.58GHz, image frequency 1.92GHz
3.3.2 Clock Jitter

<table>
<thead>
<tr>
<th>Jitter $^2$</th>
<th>SNDR</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>33.0 dB</td>
</tr>
<tr>
<td>0.009</td>
<td>32.5 dB</td>
</tr>
<tr>
<td>0.018</td>
<td>32.1 dB</td>
</tr>
<tr>
<td>0.036</td>
<td>30.7 dB</td>
</tr>
<tr>
<td>0.072</td>
<td>27.4 dB</td>
</tr>
<tr>
<td>0.108</td>
<td>24.6 dB</td>
</tr>
<tr>
<td>0.144</td>
<td>22.4 dB</td>
</tr>
<tr>
<td>0.180</td>
<td>20.5 dB</td>
</tr>
<tr>
<td>0.217</td>
<td>18.2 dB</td>
</tr>
</tbody>
</table>

$^2$ clock period variance, $\sigma$

Table 3.2: DAC noise estimations of rectangular distributed clock jitter

Another error source related to the clock is clock jitter. In contradiction to the static errors presented above, the jitter is dynamically changed at each cycle period. This was modelled as a random delay error of the arriving clock to each DAC. With a rectangular distribution of the error the maximum acceptable clock jitter variance is $\sigma = 0.072$, which can be seen in Tab. 3.2. However the jitter also contribute to the magnitude of the images outside of the spectrum, as discussed earlier. To uphold the noise margin the jitter should not exceed $\sigma = 0.009$.

3.3.3 Amplitude Mismatch

![SNDR vs DAC amplitude](image)

Figure 3.7: SNDR with respect to DAC amplitude error.

An additional mismatch issue is the difference in output amplitude levels
between the DACs. Sweeping the amplitude from 50% to 150% of one DAC, keeping the others at 100%, introduce a worst case error of 4dB. A plot of the SNDR originating from amplitude errors can be seen in Fig. 3.7. At first glance this might see harmless, but it turns out that the amplitude mismatch has the same effect on the system as the single clock skew error.

3.4 Realization

<table>
<thead>
<tr>
<th>Error type</th>
<th>Maximum tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single DAC clock skew</td>
<td>$&lt; \pm 6 %$</td>
</tr>
<tr>
<td>Multiple DAC clock skew</td>
<td>$&lt; \pm 3 %$</td>
</tr>
<tr>
<td>Clock skew of DAC pair</td>
<td>$&lt; \pm 12 %$</td>
</tr>
<tr>
<td>Clock jitter variance</td>
<td>$&lt; 0.009$</td>
</tr>
<tr>
<td>Amplitud mismatch</td>
<td>$&lt; \pm 5 %$</td>
</tr>
</tbody>
</table>

Table 3.3: DAC subsystem requirements.

The required robustness of the modelled interleaved DAC were specified by a minimum ENOB of 4 and a minimum SNDR of 26dB with all error sources combined. The previous section covered individual error sources and their impact on SNDR. Additional simulations were run to establish a set of error limits to uphold the required noise margin. The result of these simulations conclude that with all different errors combined the tolerances needs to be according to Tab. 3.3.

Commercial DACs at the time of writing reach speeds of around 2GS/s with a resolution of approximately 8 bits. With the usage of four custom built 4-bit DACs it seems achieveable to reach an effective sample rate of 14GS/s through interleaving.
Chapter 4

Noise Shaping

This chapter covers noise shaping as a mean to increase the dynamic range in the signal band, which in turn can be traded for lower requirements of the DACs. Sigma-Delta noise shaping is presented along with discussions and solutions for high speed operation of the modulator.

4.1 Concept and Theories

The previous chapter covered issues of high resolution and high sample rate conversions to the analog world. It was estimated that as low as a 4-bit DACs would be needed to reach the target frequencies. To regain the lost resolution it was suggested to use a noise shaping ΣΔ-modulator.

4.1.1 Noise Levels and Quantization

In contrast to the analog environment, the digital one has a limited resolution that varies greatly depending on its application. The limited resolution, due to quantization of the signal, results in an undesired noise floor. A more distinct signal has a deeper noise floor.

Noise originating from quantization can be seen as white noise (as long as the input is not DC or a slow varying sinusoid [9]), evenly distributed in the frequency domain. With the help of oversampling, it is possible to remove noise energy with efficient filters [6].
The noise energy in the frequency domain can be seen as the shaded areas in Fig. 4.1. Compared to Nyquist rate sampling it is possible to reduce the noise energy by a factor $M$ when oversampling with the same factor. The noise floor still has the same magnitude, which is determined by quantization and thermal noise to name two. However, with oversampling we can use a digital filter to remove noise energy outside of the signal band (illustrated by the dashed line). Noise shaping takes oversampling further by moving the in band noise out of the band, hence the expression noise shaping. The result of the noise shaping on the noise floor can be seen in Fig. 4.1c.

### 4.2 Sigma-Delta ($\Sigma\Delta$)

The $\Sigma\Delta$-modulator is a noise shaping algorithm for suppression of quantization noise in the signal band of interest. Various structures of the modulator exists with different performance characteristics and computation requirements. High performance is the most critical parameter in this thesis, whereupon low computation requirements will be the main focus.

#### 4.2.1 $\Sigma\Delta$ Structures and Behaviours

![Mathematical model of a $\Sigma\Delta$-modulator](image)
The idea behind a $\Sigma\Delta$-modulator is to quantize the data in a controlled manner by first integrating the signal, quantize it, and finally restore it by differentiation. The quantization can be seen as noise and because it is added after the integrator it is only differentiated. A mathematically equivalent schematic can be seen in Fig. 4.2.

A corresponding schematic for digital implementation with adders and subtractors is shown in Fig. 4.3, where $X(z)$ is the input signal, $E(z)$ is quantization noise and $Y(z)$ is the output signal. From these schematics we can extract the functions for $Y(z)$ and $W(z)$, resulting in equations 4.1a and 4.1b.

$$Y(z) = W(z) + E(z) \quad (4.1a)$$

$$W(z) = z^{-1}X(z) - z^{-1}Y(z) + z^{-1}W(z) \Leftrightarrow (1 - z^{-1})W(z) = z^{-1}(X(z) - Y(z)) \Leftrightarrow W(z) = \frac{z^{-1}(X(z) - Y(z))}{1 - z^{-1}} \quad (4.1b)$$

By combining Eq. 4.1a and 4.1b a new expression for $Y(z)$ is achieved, shown in the following equations.

$$Y(z) = \frac{z^{-1}(X(z) - Y(z))}{1 - z^{-1}} + E(z) \Leftrightarrow (1 - z^{-1})Y(z) = z^{-1}(X(z) - Y(z)) + (1 - z^{-1})E(z) \Leftrightarrow Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \quad (4.2)$$

It’s common to divide $Y(z)$ into two functions, namely the signal transfer function (STF) and the noise transfer function (NTF). These calculations are shown in Eqs. 4.3a and 4.3b.
\[ Y(z) = STF(z)X(z) + NTF(z)E(z) \]
\[ STF(z) = z^{-1} \quad (4.3a) \]
\[ NTF(z) = 1 - z^{-1} \quad (4.3b) \]

We are interested in analysing the NTF and its behaviour in the frequency domain. For this purpose the following substitutions are of interest; \( z = e^{j\omega} \), \( \omega = 2\pi f \). To study the magnitude response we calculate the square of the NTF in the following way.

\[
|1 - z^{-1}|^2 = |1 - e^{-j\omega}|^2 \\
= |1 - \cos(\omega) - j \sin(\omega)|^2 \\
= \left(\sqrt{(1 - \cos(\omega))^2 + (\sin(\omega))^2}\right)^2 \\
= (1 - \cos(\omega))^2 + \sin^2(\omega) \\
= 1 - 2 \cos(\omega) + \cos^2(\omega) + \sin^2(\omega) \\
= 2 - 2 \cos(\omega) \\
= 4 \sin^2\left(\frac{\omega}{2}\right) \\
= (2 \sin(\pi f))^2 \quad (4.4)
\]

From Eq. 4.4 we can specifically see that the NTF is 0 at \( f = 0 \) and in general has a high pass characteristic.

The frequency spectrum of a quantized signal compared to a \( \Sigma\Delta \)-modulated signal with its characteristic shape can be seen in Fig. 4.4.

### 4.2.2 SNR and Quantization Considerations

In most cases, the decisive factor when designing a system with a \( \Sigma\Delta \)-modulator is to adjust the oversampling rate of a fixed architecture to meet the requirements. For our application there is little room for increasing the oversampling rate while it is possible to change the architecture of the modulator and output resolution instead. Design parameters of the \( \Sigma\Delta \)-modulator includes higher order modulator and multi-bit quantization.
4.2 Sigma-Delta ($\Sigma\Delta$)

High Order Modulation

By using a higher-order modulator it is possible to trade a more efficient noise shaping algorithm for higher complexity and modulator stability. To keep both these issues under control, the tested setups were constructed by several cascaded first order modulators, effectively forming a so called multi-stage modulator.

Multi-bit Quantization

The level of quantization is another design parameter of the modulator. Less quantization results in less loss in signal quality while a higher degree results in more relaxed requirements on the DACs.

Simulations

A set of models were created in MATLAB to evaluate the differences between various combinations of modulator order and quantization levels. The input to each modulator consisted of an ideal sinusoid quantized to 6 bits. The ability to suppress noise is measured in SNDR and a greater value is an indication of better performance. The results of the simulations are presented in Tab. 4.1.
### Table 4.1: $\Sigma\Delta$ noise levels with respect to modulator order and quantization.

<table>
<thead>
<tr>
<th>Modulator order</th>
<th>3-bit</th>
<th>4-bit</th>
<th>5-bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>32.3 dB</td>
<td>37.7 dB</td>
<td>41.4 dB</td>
</tr>
<tr>
<td>2</td>
<td>36.2 dB</td>
<td>40.3 dB</td>
<td>42.4 dB</td>
</tr>
<tr>
<td>3</td>
<td>38.8 dB</td>
<td>41.4 dB</td>
<td>42.8 dB</td>
</tr>
<tr>
<td>4</td>
<td>40.2 dB</td>
<td>42.6 dB</td>
<td>43.1 dB</td>
</tr>
<tr>
<td>5</td>
<td>41.8 dB</td>
<td>42.9 dB</td>
<td>43.1 dB</td>
</tr>
</tbody>
</table>

Due to the low oversampling rate the gain of higher modulator order and less quantization is reduced. Both higher modulator order and quantization puts greater strain on the computation path, which will be discussed in the next section. The simulations indicates room for improvements in noise levels if the additional computation resources are achievable.

### 4.2.3 Retiming

It is possible to retime a circuit by introducing additional delay elements at the input or output of the system without changing its properties [7]. Due to the layout of the $\Sigma\Delta$, it is not possible to reduce the critical path through strict retiming. However, by increasing the delay of the already present delay element to two clock cycles, it is possible to reach the structure in Fig. 4.5 which only has one adder in the critical path. This changes the characteristics of the system, similar to interpolation, as can be seen in Fig. 4.7, compared to the characteristics of the original modulator, seen in Fig. 4.6. The spectrum is compressed and effectively moving noise back into the signal band, removing much of the noise shaping property. Thus, retiming was discarded as a solution.
Figure 4.6: Frequency spectrum of original \( \Sigma\Delta \)

Figure 4.7: Frequency spectrum of retimed \( \Sigma\Delta \)
4.2.4 Interleaving

Interleaving is a method of using two duplicated execution paths, each calculating every other data sample at half the speed. Using up to four interleaved paths to match the number of DACs were suggested in the proposed solution. Previously implemented time-interleaved solutions of ΣΔ-modulators [5, 3, 4] only increase the noise shaping effect at the same operating frequency compared non-interleaved counterpart. The trade-off is a greater strain on the computations, as a result of a longer critical path. This is because each sample is related to the previous sample and even though the data path is split into multiple ones they still need to be interconnected for proper noise shaping. To conclude on these attempts, there is no way to apply pipelining or time interleaving to the ΣΔ-modulator because of its recursive nature [4].

4.2.5 Oversampling Reduction

To further exhaust the possibilities of using a noise shaper in the system, the idea of reducing the oversampling from 4 to 2 emerged. However, the noise shaping effect proved to be very limited at this oversampling rate, effectively worse than pure quantization. Looking back at the previously discussed NTF in section 4.2.1, the lowest oversampling rate can be calculated the following way

\[(2 \sin(\omega/2))^2 = 1\]
\[\sin(\omega/2) = \frac{1}{2}\]
\[\omega = \frac{\pi}{3}\]

(4.5)

An OSR of 4 and 2 allows normalized frequencies up to π/4 and π/2 respectively. Thus, according to Eq. 4.5, the minimum OSR is 3. This means that an oversampling rate of 2 will cause the ΣΔ-modulator to amplify quantization noise of frequencies between π/3 and π/2.

4.2.6 Non-feedback ΣΔ

An alternative to the fundamental ΣΔ architecture was presented by D. Wisland et. al. in [8]. By using modulo arithmetics and a special quantizer
4.2 Sigma-Delta (ΣΔ)

Figure 4.8: First order non-feedback ΣΔ schematic

function, the global feedback in the ΣΔ could be discarded. It was also realized that the architecture is scalable with no extra penalty in terms of computational load. Higher order modulators are created by adding additional accumulators and differentiators at each side of the quantizer. Since there is no global feedback it is possible to pipeline the structure efficiently by introducing pipelining registers between each block. The critical path limitation is the delay of one adder regardless of modulator order [1].

Modulo arithmetics and quantization

The theoretical implementation of the non-feedback ΣΔ-modulator requires infinite accumulators which is not feasible for a real implementation. A solution based on modulo arithmetic was suggested by D. Wisland, where the accumulators over and underflow in a controlled manner.

\[
H_{\text{acc}}(z) = \frac{1}{1 - z^{-1}} \quad (4.6a)
\]

\[
H_{\text{diff}}(z) = 1 - z^{-1} \quad (4.6b)
\]

As can be seen in Fig. 4.8, the non-feedback ΣΔ-modulator solution uses an accumulator, a quantizer and a differentiator. The transfer function is expressed in Eq. 4.6a and is indeed a simple accumulator. The input data resolution to the accumulator is 6 bits, resulting in an integer range of \([-32 : 1 : 31]\]. Values outside of the range is over- or underflowed in a regular two’s complement fashion.

\[
v(n) = u(n) - \text{mod}(u(n), 2^{i-j}) \quad (4.7)
\]

Equation 4.7 is the quantizer function which reduces the resolution of the signal. \(u(n)\) is the input signal to the quantizer block as shown in Fig. 4.8 and \(v(n)\) is the output signal. \(i\) and \(j\) are the resolutions in bits of the input and output signal respectively. The mod-function is the built in modulus
function in MATLAB which is used to reduce the resolution of the output signal to \( j \) bits, effectively resulting in the integer range of \([-32 : 4 : 28] \). Finally, the signal is differentiated according to the Eq. 4.6b.

To better understand how the non-feedback \( \Sigma \Delta \) works it is a good idea to investigate what the different signal values are at different stages of the modulator. In this example the input to the modulator is a DC signal with amplitude 7. The output of the accumulator is shown in Fig. 4.9b and we can see that it overflows when it reaches 31 and starts over at -32. The output from the quantizer (4.9c) is of lower resolution and has the same appearance as the output of the accumulator. Finally, the signal is differentiated and the result is displayed in Fig. 4.9d. Since the signal is quantized, the value 7 can not be represented correctly and is instead represented by the mean value of the output. Studying the output signal more closely reveals that it has three 8’s and one 4 in each section of four values and the average equals to the input value of 7.

Figure 4.9: Signal values at different stages of the non-feedback \( \Sigma \Delta \). a) input signal, b) output from accumulator, c) output from quantizer, d) output from differentiator.
4.2 Sigma-Delta (ΣΔ)

Stability

The non-feedback modulator exhibits the same issues regarding stability as the fundamental modulator. To be able to use a full range input signal the accumulator is designed to use one guard bit, thus having a range of $[-64 : 1 : 63]$. To retain proper functionality, the differentiator needs to use the same kind of over- and underflowing as the accumulator. Hence, it uses one guard bit as well, increasing its effective range to $[-64 : 4 : 60]$.

Hardware Implementation

While the methods to create a model of the ΣΔ-modulator that resembles the functionality in hardware seems tricky, it is far more easy in hardware. The modulo arithmetics logic consists of standard adders that over- or underflow thanks to the way two’s complement binary calculation is constructed. Both the accumulator and the differentiator use the same type of hardware with the difference that the differentiator adder is used as a subtractor by simply inverting the pins from the register and setting the carry in input to 1. The quantizer function is just a matter of not connecting the least significant bits from the accumulator to the differentiator.
Chapter 5

Filtering

At different stages of the system different kind of filtering is needed. When the signal is upsampled at the input, an interpolation filter is needed. Furthermore, to reduce inter symbol interference a raised cosine filter will be added.

5.1 Interpolation filter

The input sampling rate to the system is 3.5GS/s and to be able to use noise shaping efficiently the signal needs to be upsampled. For our application it was decided that an over sampling rate of 4 was suitable. The time domain behaviour of the signal during the upsampling and filtering can be seen in Fig. 5.1.

5.2 Raised Cosine filter

The idea of the raised cosine filter is to reduce the interference between sequential symbols in a communication link [2]. This is achieved by using a filter that has as much energy as possible in the main lobe, zero crossings at main lobes of other symbols and rapidly decaying amplitude outside of its own pulse interval. Raised cosine filters are used in various communication systems, for example W-CDMA.

Theoretically, to limit the intersymbol interference, the combined filtering effect of the entire system should be of a raised cosine type. It is common practice to divide this filter into two filters, one at the sender side and one
Figure 5.1: a) Input signal, 3.5GS/s, b) Four times upsampling, 14GS/s c) Interpolation filtering, 14GS/s.

Figure 5.2: Coefficients for a 16 taps FIR based RRC filter
at the receiving side of the link. The resulting filters are root raised cosine (RRC) filters who create the raised cosine effect when cascaded. The filter characteristics can be seen in Fig. 5.2.

The interpolation filter and the RRC filter are in reality both low pass filters, which can be combined into one single filter. An effective filter structure for digital implementation that also is easy to parallelize is the FIR structure, thus making it attractive for a high data rate environment.
Chapter 6

Algorithm Conclusions

This section covers conclusions drawn from results of model simulations and discusses the feasibility of the proposed solution.

6.1 Parallel DAC

The proposed setup with four parallel DACs, operating with a clock offset of $\pi/2$ proved to work well. The structure needs to maintain a set of requirements regarding the clocking and mismatch. Special care need to be taken regarding clock skew which already at small variations from the ideal case introduce interleaving images outside of the signal band. The alternative to suppress these images with analog filters is not feasible due to the its required steepness.

6.2 Sigma Delta-modulator

Many different methods for a parallel noise shaping architecture was investigated. It was concluded that previous attempts to parallelize a $\Sigma\Delta$-modulator increase the critical path when the computational frequency is reduced. To reduce the critical path, another $\Sigma\Delta$-structure with no global feedback was tested with good results. Without a global feedback the critical path is reduced from two adders of the fundamental $\Sigma\Delta$ to one of the non-feedback $\Sigma\Delta$. Another positive property of the non-feedback version is that it is scalable without increasing the critical path. The most promising solution for the intended application was concluded to be a higher order non-feedback $\Sigma\Delta$ operating at the high data rate.
6.3 Filters

The digital filtering consists of an RRC-filter which also act as a interpolation filter. Both filters are of low pass character and realized by the fundamental FIR structure. The interpolation filter is needed because of the upsampling and by using coefficients wisely the result is an RRC-filter that reduce the probability of interference between symbols.
Chapter 7

Measurements

Measurements are conducted to verify the functionality and performance of the interleaved DAC structure and the \( \Sigma \Delta \) noise shaping algorithm. As a result of the conclusions drawn from the algorithm development, the main focus of the measurements is to characterize the performance of the interleaved DAC and not so much about \( \Sigma \Delta \) noise shaping.

7.1 Algorithm porting to Verilog

This section covers the transformation of the algorithm from the MATLAB environment into a hardware description language and further on testing of the algorithm on a SP Devices custom evaluation board.

7.1.1 HDL blocks

The structure of the design can be seen in Fig. 7.1. The on-chip RAM is fed with data from a PC over a USB interface. Once a data set is loaded
into the memory the algorithm is started and the $\Sigma\Delta$-block retrieves data from the RAM.

![Sigma Delta Block Diagram](image.png)

Figure 7.2: $\Sigma\Delta$ structure

Thanks to the scalability of the non feedback $\Sigma\Delta$ it was constructed as three simple blocks; accumulator, quantizer and differentiator. Figure 7.2 shows the structure of a second order $\Sigma\Delta$. Higher order modulators are created by adding accumulators and differentiators at their respective positions of the quantizer. For this setup, a second order $\Sigma\Delta$-modulator was realized.

### 7.1.2 Simulation

Simulation was carried out to verify proper operation of the $\Sigma\Delta$-modulator as well as operating instructions to the functionality of the entire board. The simulation environment was Xilinx’s ISE Simulator and the output was compared to the MATLAB model.

### 7.2 Evaluation board

The final solution needs to be implemented on silicon to be able to reach the specified frequencies. However, it is possible to characterize the algorithm and DAC function at lower frequencies. For this evaluation it was decided to use a custom made PCB with two DACs.

### 7.2.1 DAC Structure

Instead of using four RTZDACs, which properties are suited for high speed operation, it is possible to use two normal DACs where the previous zero-cycle of output one and two are replaced with the on-cycle of output 3 and 4. By doing this its possible to evaluate the interleaving idea with only two DACs.
7.2 Evaluation board

Figure 7.3: DAC Structure

Figure 7.4: Dual DAC evaluation board

Figure 7.5: ADQ114 data acquisition board
7.3 Measurement setup

The evaluation board has a Xilinx Virtex5 FPGA capable of 550MHz clock rate, but to suit the overall test bench a more conservative operating frequency of 400MHz was used. Both DACs are connected in parallel and fed data at the same time. To achieve the $\pi/2$ offset between the DACs, each sample was extended to cover two output cycles, whereupon the samples to the second DAC was delayed one clock cycle. The effective sample rate is reduced to 200MS/s, but by running the DACs interleaved is should be possible to reach the equivalent of 400MS/s. In this way it adds the possibility to compare the results to the ideal case of a single DAC at 400MS.

Finally, the two outputs are combined and connected to a SP Devices data acquisition card which is capable of measuring the high frequency signal.

7.4 DAC Measurements

7.4.1 400MS/s Operation

![Figure 7.6: Single 400MS/s DAC](image)

Figure 7.6 displays a zoomed in frequency spectrum view of a single 400MS/s DAC and Fig. 7.7 displays the corresponding view of two 200MS/s DACs operating time-interleaved.

<table>
<thead>
<tr>
<th></th>
<th>Ideal</th>
<th>Interleaved</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNDR</td>
<td>31.6 dB</td>
<td>31.7 dB</td>
</tr>
</tbody>
</table>

Table 7.1: DAC measurements

In band noise measurements is shown in Tab. 7.1 and it demonstrates only a slight performance difference between a single 400MS/s DAC and two
200MS/s interleaved DACs. The reason for the better SNDR value of the interleaved setup is due to the behaviour of the parallel DACs, presented in section 3.1.

### 7.4.2 800MS/s Operation

A further proof of concept is to test the interleaved DAC setup operating at full speed. To achieve the desired $\pi/2$ between the DACs, the length of the cables between the DAC board and the ADC board was altered. By extending the cable from the second DAC by a length equalling to a half sample period, an $\pi/2$ phase offset is attained. According to the theory in section 3.3, the unwanted images close to the signal band should not appear since DAC1 and DAC3 is in fact the same DAC in this setup. However, interleaving images due to skew between the DACs, which is a result of different cable lengths, will still be present.

<table>
<thead>
<tr>
<th></th>
<th>22cm</th>
<th>27cm</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNDR</td>
<td>30.3 dB</td>
<td>30.4 dB</td>
</tr>
</tbody>
</table>

Table 7.2: Two 400MS/s interleaved DACs

The tests conducted at full speed prove close to identical results of 30.3dB and 30.4dB in band SNDR with cable extensions of 22cm and 27cm respectively. The out of band images that can be seen in Fig. 7.8 and 7.9 clearly shows the differences in amplitude as a result of imperfect phase offset between the DACs.
Figure 7.8: Two 400MS/s interleaved DACs, 22cm cable extension

Figure 7.9: Two 400MS/s interleaved DACs, 27cm cable extension
7.4 DAC Measurements

7.4.3 QAM

In contrast to testing with strictly sinusoids, measurements were also conducted with 16QAM-data from a communication link model. The test setup consisted of 16QAM-data upsampled two times, followed by two interleaved DACs and finally an ADC. The combined analog oversample rate of the DAC and ADC was four.

![QAM Diagram](image)

Figure 7.10: Transmission of 16QAM-data on an interleaved DAC structure.

The blue dots correspond to a correctly received symbol, while a red dot indicates a faulty symbol. In an ideal case, the dots should all be blue and closely centered around the cyan colored dots which represents all possible symbols of 16QAM-data. The error rate displayed above is not acceptable for a real system, but tuning for this specific task is not within the scope of this thesis.
Chapter 8

Conclusions

This chapter concludes the different parts of the thesis work by

- Concluding the algorithm development from section 3.1 and 4.2.
- Summarizing the measurements conducted in section 7.4.

8.1 Algorithm conclusions

The aim of this thesis was to examine the possibilities of interleaving DACs to achieve higher output bandwidths. To reach even higher speeds, digital noise shaping was investigated to be able to reduce the number of bits in the DACs.

8.1.1 DAC interleaving

The idea of time interleaving multiple DACs to reach higher output bandwidths proved to work well both in a model environment and in reality. Special cautions need to be taken regarding clock alignment of a real implementation. Further errors such as amplitude mismatch and jitter was modelled with the conclusion that a real implementation is feasible if the margins presented in section 3.4 are upheld.

8.1.2 Digital Noise Shaping

Noise shaping of the signal to the DACs with a $\Sigma\Delta$ architecture proved to be successful in theory. However, the main goal of parallelizing the modu-
lator to be able to reach the target frequencies proved to be unsuccessful. Previous attempts to make the architecture more parallel have the drawback of increasing the computational load, effectively rendering it unusable for the intended application. The most promising solution evaluated was a non-feedback modulator, using only a single adder in its critical path, but still requiring operation at the oversampled data rate. Overall, the use of a $\Sigma\Delta$-modulator in this environment is not extensively useful due to limited oversampling and parallelization possibilities.

8.2 Measurement conclusions

The proposed solution of four DACs is sensitive to clock skew, resulting in unwanted image frequencies outside of the signal band. The measured setup consisting of two DACs is immune to this error which leads to the conclusion that when comparing RTZDACs to normal DACs, the latter is less prone to interleaving errors.

Measurements conducted on an evaluation board confirmed the operation of two DACs interleaved. At low speed testing, the interleaved solution displayed practically identical results compared to a single DAC. High speed operation further proved the possibilities to double the output frequency with DAC interleaving.
Bibliography


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